R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example on page 6 lines 8-10, page 7 Table 1, page 7 lines 18-20, page 9 lines 1-2 and FIGS. 2-4, as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2, 4-11 and 13-19 under 35 U.S.C. §102(b) as being anticipated by Uchida et al. '304 (hereafter Uchida) has been obviated by appropriate amendment and should be withdrawn.

Uchida discloses a semiconductor integrated circuit (Title). Claim 1 provides a plurality of configuration pins configured to receive a plurality of configuration signals generated external to an apparatus. The bonding option pads 6 and 7 of Uchida do not appear to be coupled to configuration pins to receive configuration signals generated external to the circuit. Therefore, Uchida does not appear to disclose or suggest a plurality of configuration pins configured to receive a plurality

of configuration signals generated external to an apparatus as presently claimed.

Claim 1 further provides a first logic gate configured to generate a first identification signal from a plurality of configuration signals and a first multiplexer directly connected to the first logic gate to multiplex the first identification signal to a first multiplexer output. In contrast, Uchida appears to be silent regarding a first multiplexer directly connected to a first logic date. Therefore, Uchida does not appear to disclose or suggest a first logic gate configured to generate a first identification signal from a plurality of configuration signals and a first multiplexer directly connected to the first logic gate to multiplex the first identification signal to a first multiplexer output as presently claimed.

Claim 1 further provides a shift register couplable to an input pin. In contrast, in ID register 5 shown in FIGS. 1, 2 and 5-8 of Uchida is not shown being couplable to any pin. Therefore, Uchida does not appear to disclose or suggest a shift register couplable to an input pin as presently claimed. Independent claims 13 and 14 provide language similar to claim 1. As such, claims 1, 13 and 14 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides that the configuration signals are user variable. In contrast, column 5, lines 22-26 of Uchida disclose

that the bonding option pads 6 and 7 are either bonded to ground pins or left floating. Therefore, the configuration signals disclosed by Uchida appear to be fixed. Therefore, Uchida does not appear to disclose or suggest configuration signals that are user variable as presently claimed. As such, claim 2 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 5 provides that a device identification determines a storage capacity of a circuit. In contrast, Uchida appears to be silent regarding a variable storage capacity of the circuit. Therefore, Uchida does not appear to disclose or suggest that a device identification determines a storage capacity of a circuit as presently claimed. As such, claim 5 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 6 provides a second multiplexer directly connected to a second logic gate and to a second memory element of a shift register to generate a second identification signal that forms a second portion of a device identification. In contrast, Uchida appears to be silent regarding a second multiplexer directly connected to a second logic gate and to a second memory element of a shift register. Therefore, Uchida does not appear to disclose or suggest a second multiplexer directly connected to a second logic gate and a second memory element of a shift register to generate a second identification signal that forms a second portion of a

device identification as presently claimed. As such, claim 6 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 8 provides that the second logic gate performs a NAND operation on the configuration signals. In contrast, Uchida appears to be silent regarding NAND operations. Therefore, Uchida does not appear to disclose or suggest that a second logic gate performs a NAND operation on a plurality of configuration signals as presently claimed. As such, claim 8 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 9 provides that the circuit further comprises a FIFO memory. Despite the assertion on page 3, item 15 of the Office Action, both column 9 and FIG. 7, and the remaining sections of Uchida appear to be silent regarding a FIFO memory. Therefore, Uchida does not appear to disclose or suggest a circuit further comprising a FIFO memory as presently claimed. As such, claim 9 is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 3, 12 and 20 under 35 U.S.C. §103(a) as being unpatentable over Uchida in view of the Background section of the pending application has been obviated by appropriate amendment and should be withdrawn.

Claims 3, 12 and 20 depended either directly or indirectly from independent claims 1 or 14, which are now believed to be allowable. As such, claims 3, 12 and 20 are fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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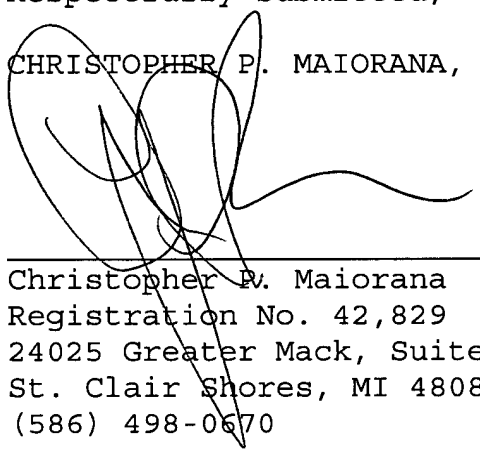

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